FIG. 1

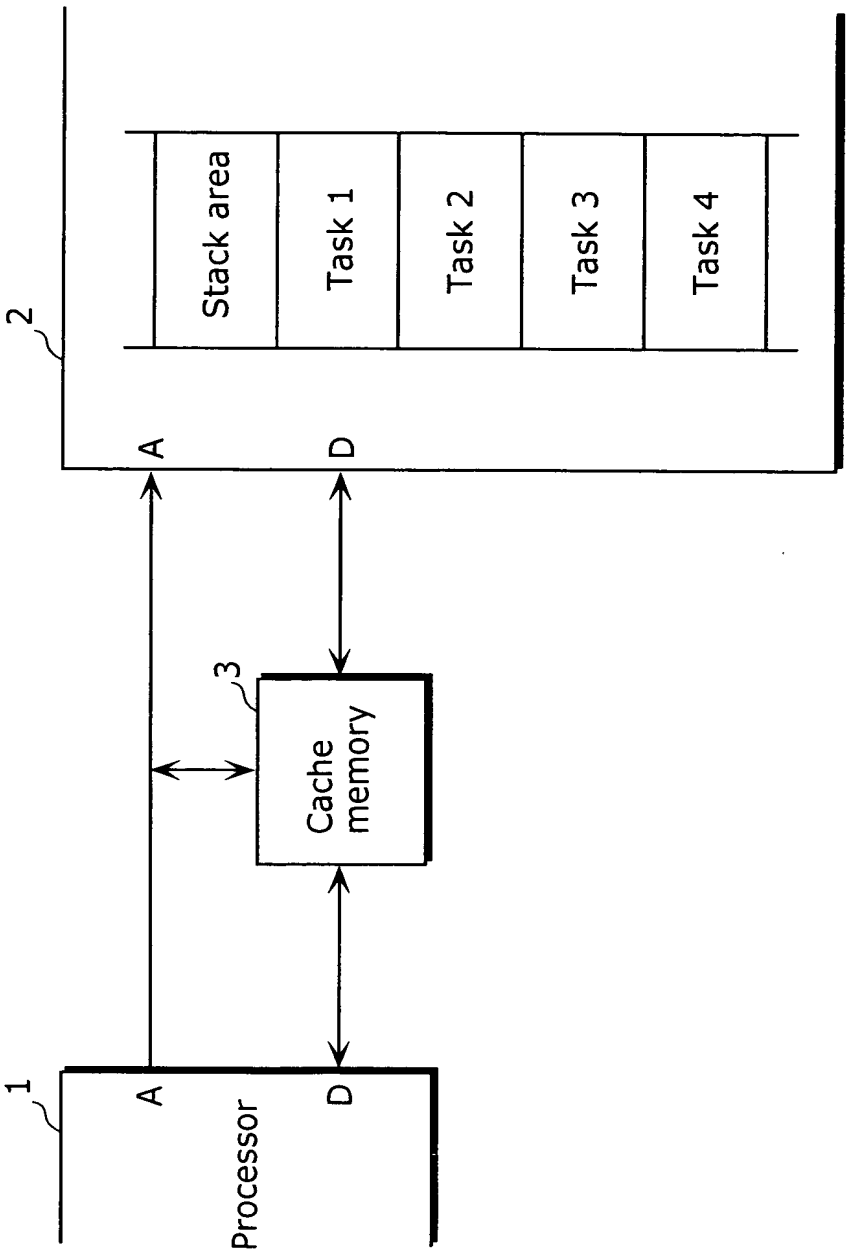
1
Processor
A
D
3
Cache memory
2
Stack area
Task 1
Task 2
Task 3
Task 4
A
D

FIG. 2

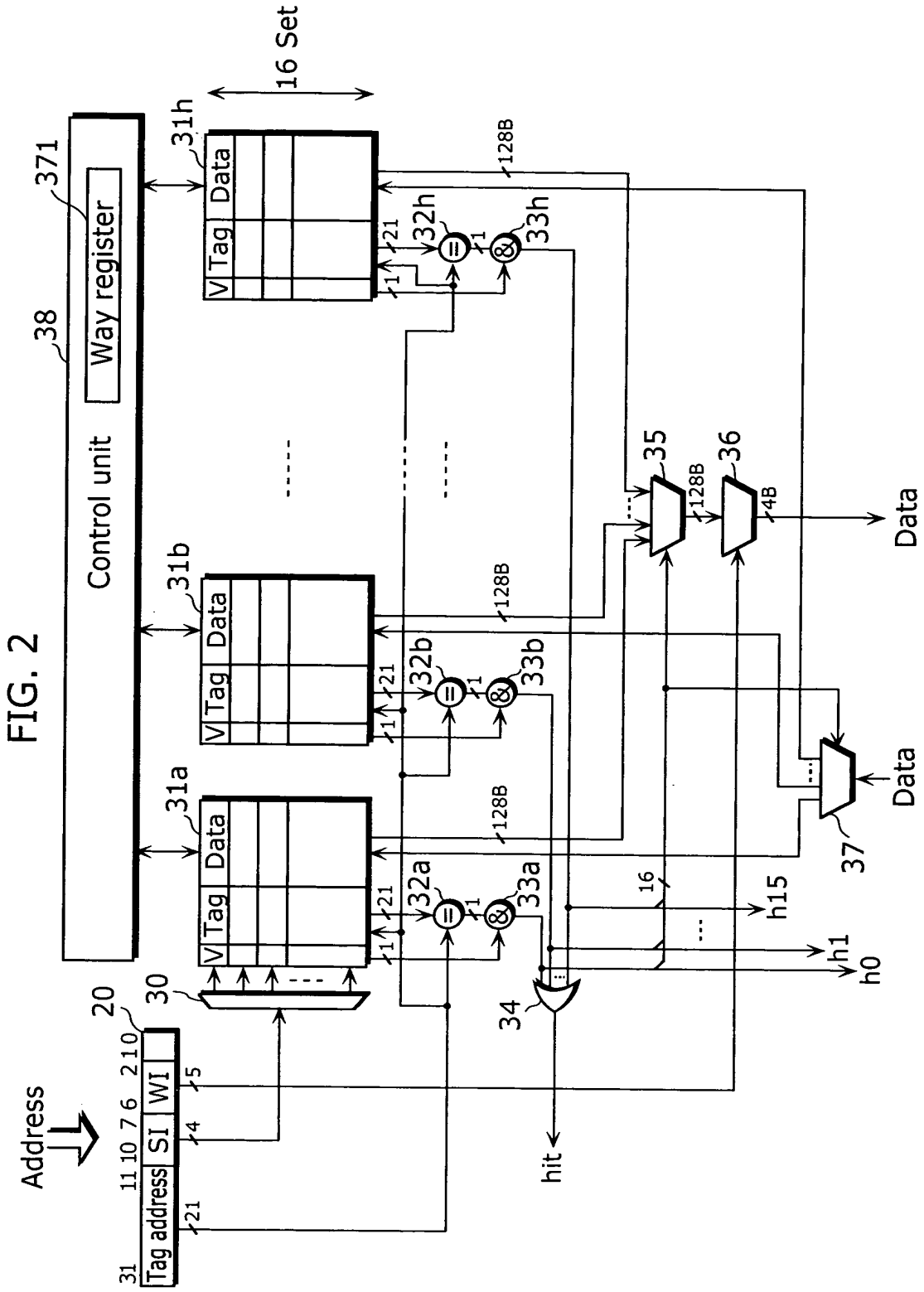
16 Set
371
Way register
38
Control unit
31h
31b
31a
Data
V
Tag
128B
21
1
32h
32b
32a
33h
33b
33a
35
36
37
4B
Data
h15
h1
h0
16
34
hit
30
20
Address
Tag address
SI
WI
11 10 7 6 2 1 0
31
5
4

FIG. 3

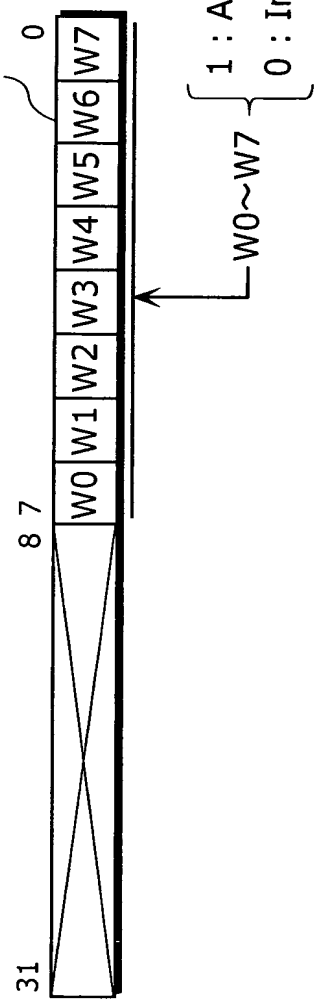
371
0
W7
W6
W5
W4
W3
W2
W1
W0
8 7
31
W0~W7
1 : Active way
0 : Inactive way

FIG. 4

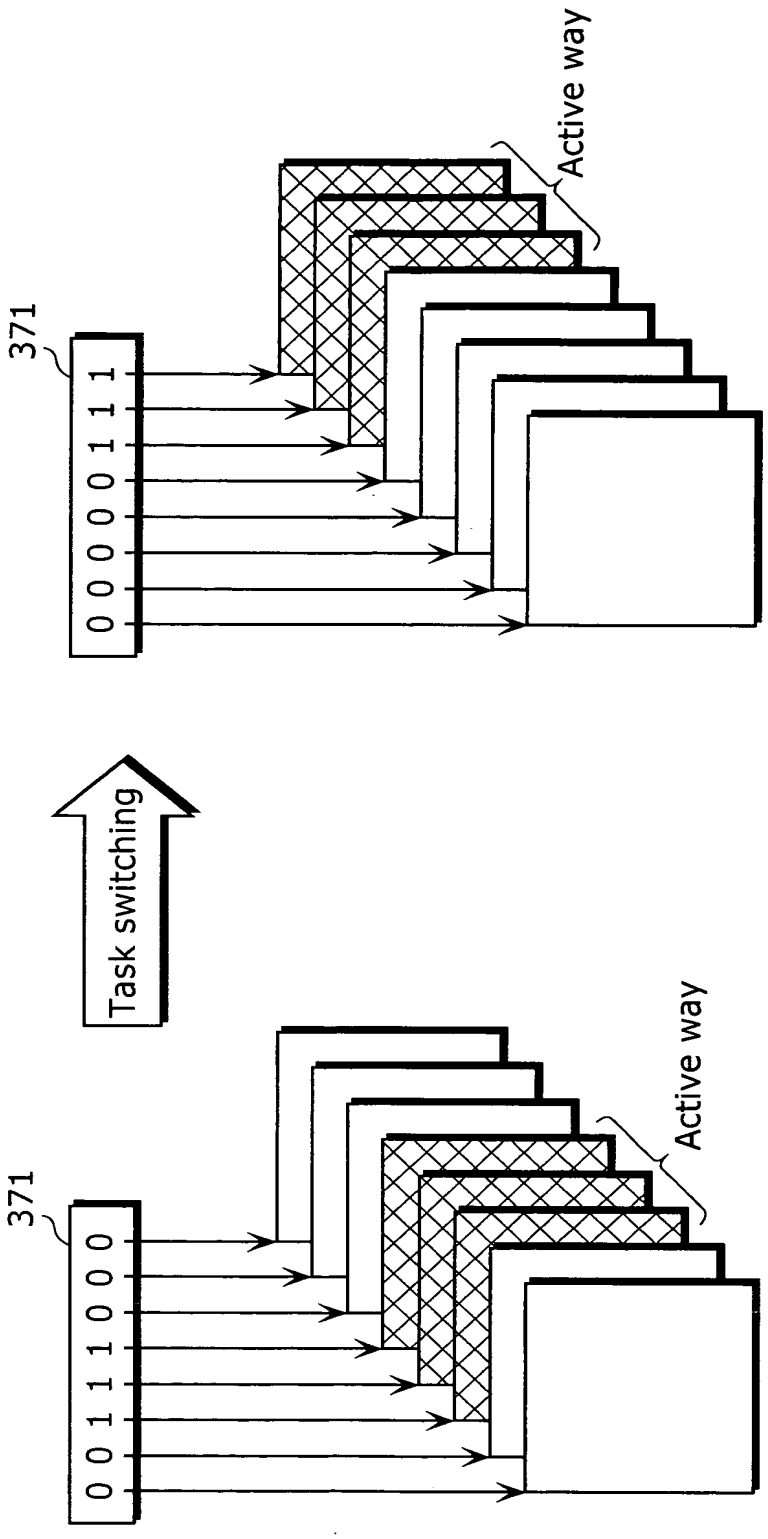
371
0 0 0 0 0 1 1 1
Active way
Task switching
371
0 0 1 1 1 0 0 0
Active way

FIG. 5

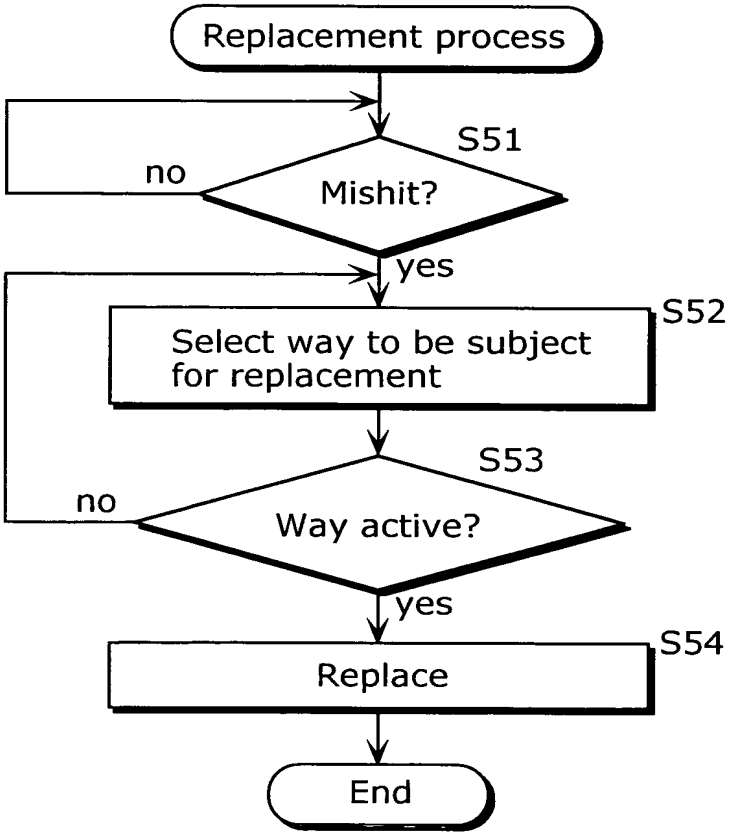
Replacement process
S51
Mishit?
no
yes
S52
Select way to be subject for replacement
S53
Way active?
no
yes
S54
Replace
End

FIG. 6

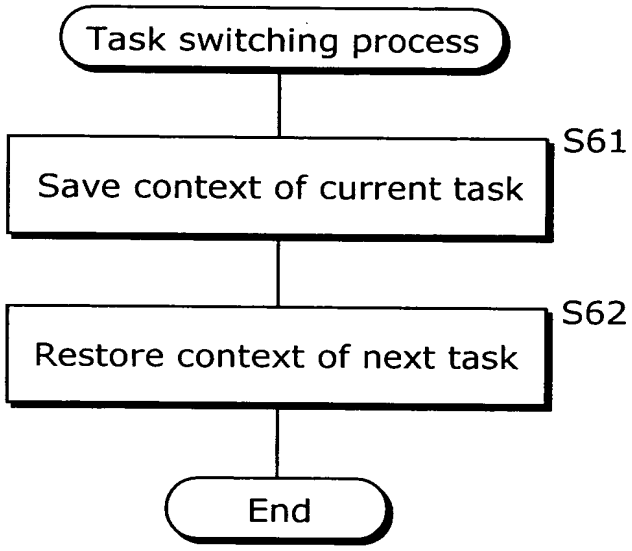
Task switching process
S61
Save context of current task
S62
Restore context of next task
End

FIG. 7

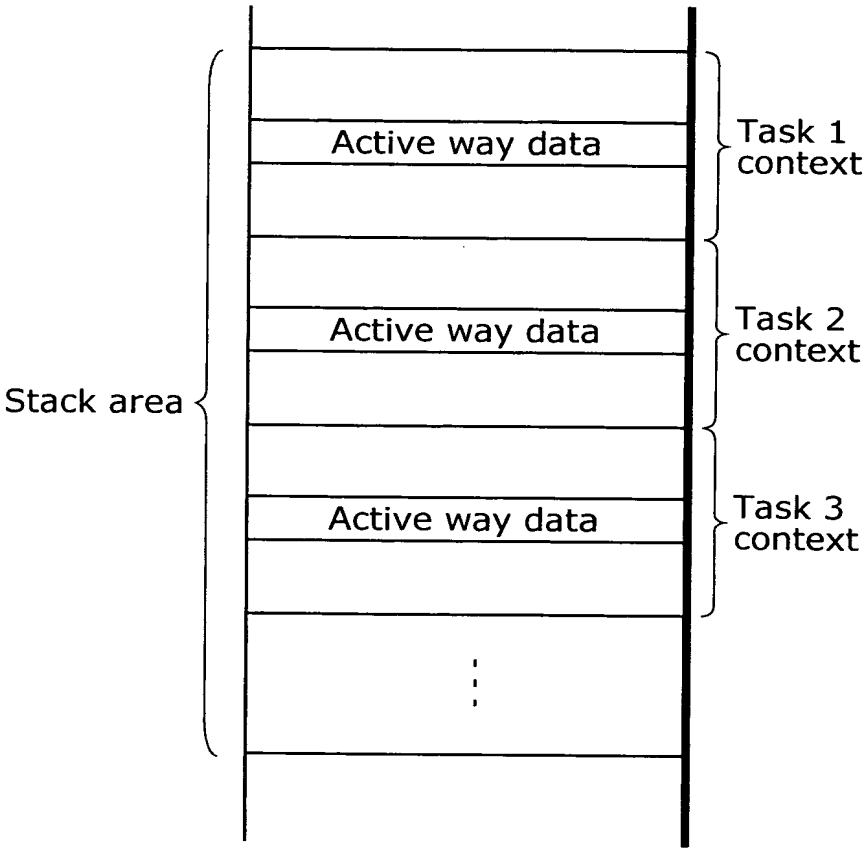
Active way data
Active way data
Active way data
Stack area
Task 1 context
Task 2 context
Task 3 context

FIG. 8

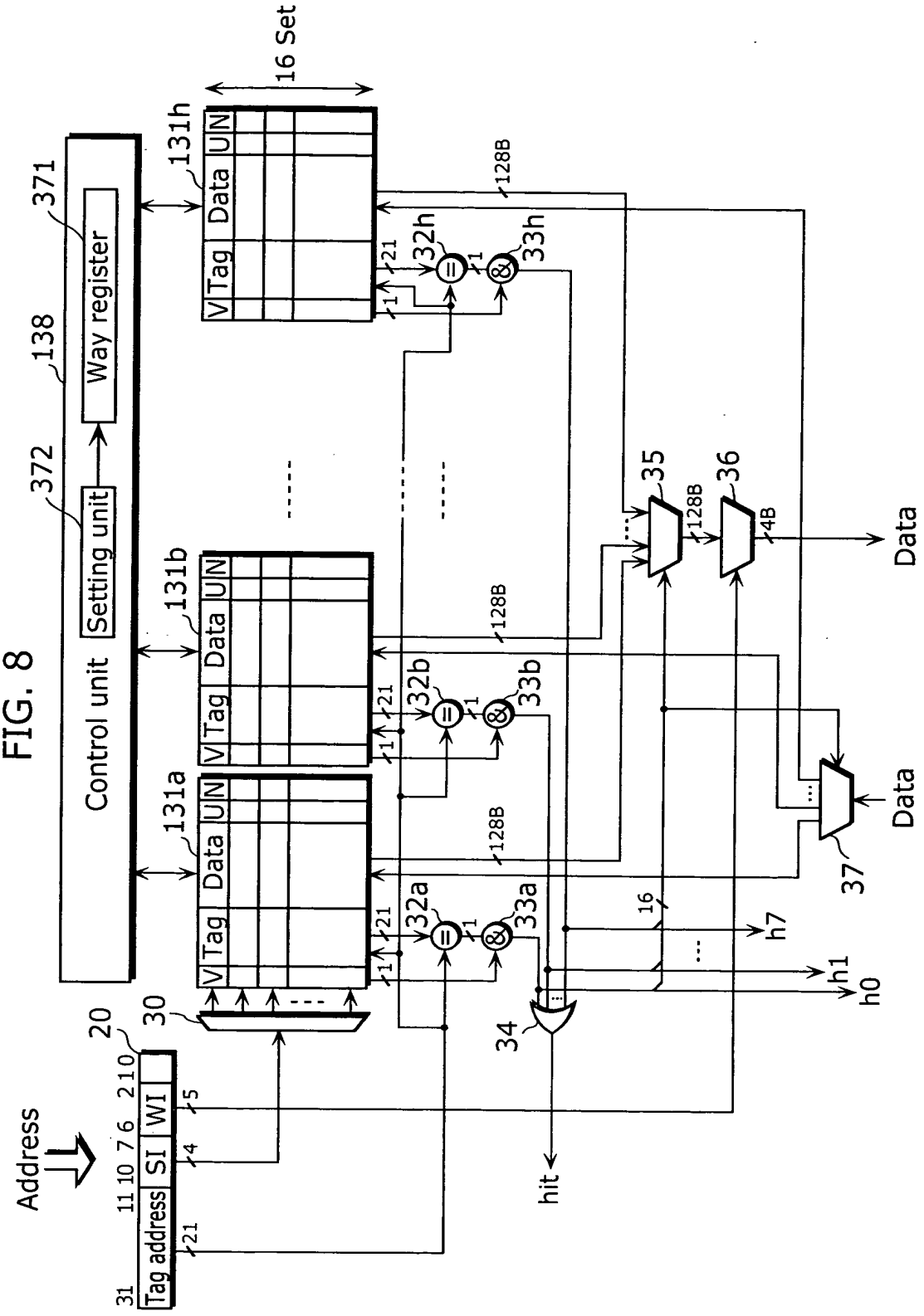
Address
Tag address
SI
WI
Control unit
Setting unit
Way register
16 Set
V
Tag
Data
U
N
hit
Data
h0
h1
h7

FIG. 9

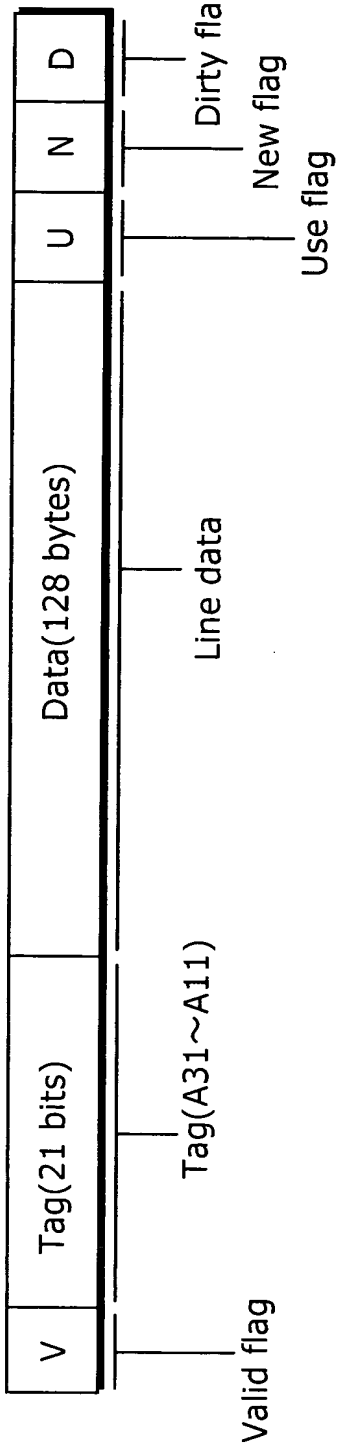
V
Tag(21 bits)
Data(128 bytes)
U
N
D
Valid flag
Tag(A31~A11)
Line data
Use flag
New flag
Dirty flag

FIG. 10

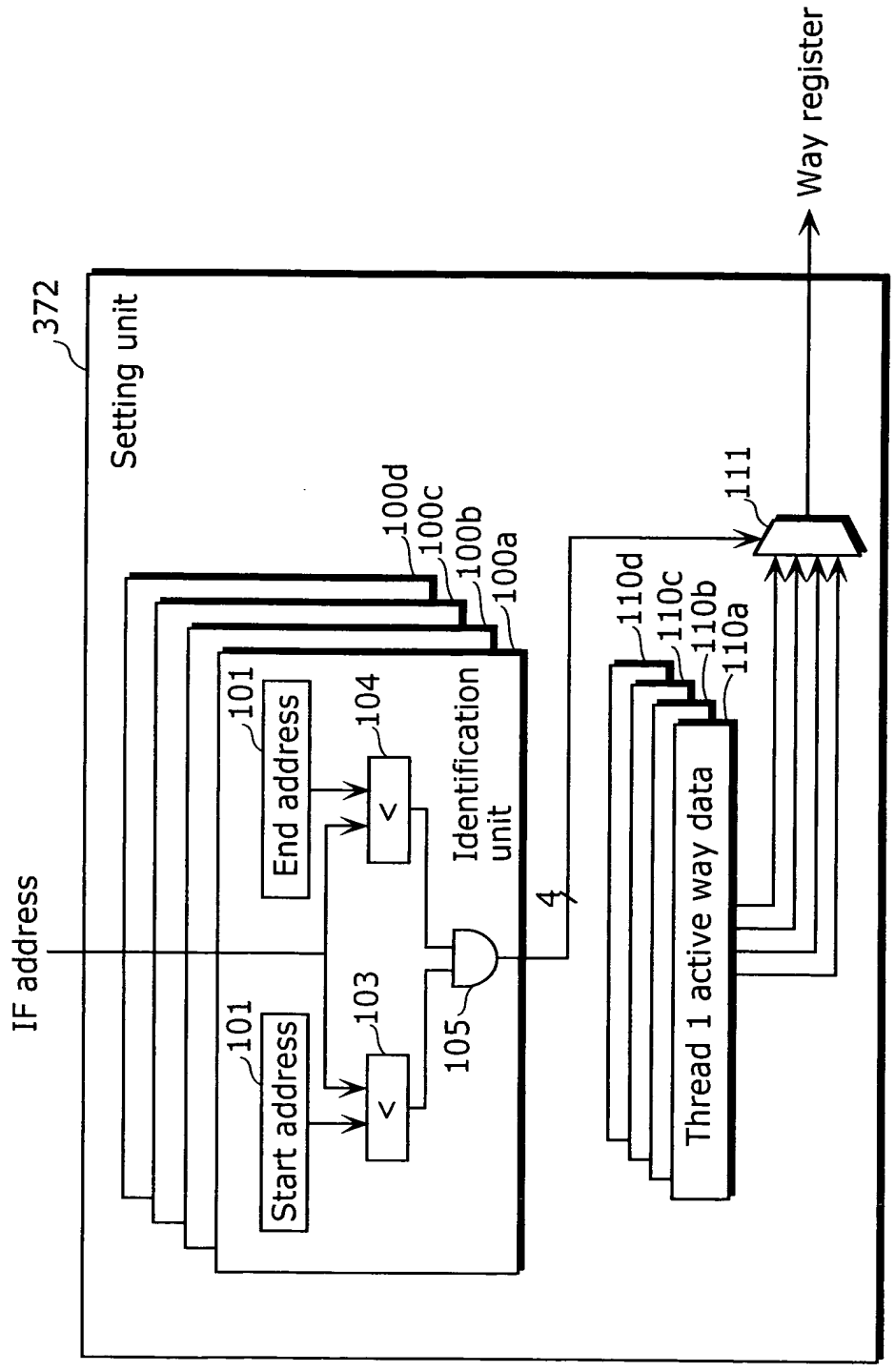
372
Setting unit
IF address
Start address
End address
101
101
103
104
105
Identification unit
100a
100b
100c
100d
4
110a
110b
110c
110d
Thread 1 active way data
111
Way register

FIG. 11

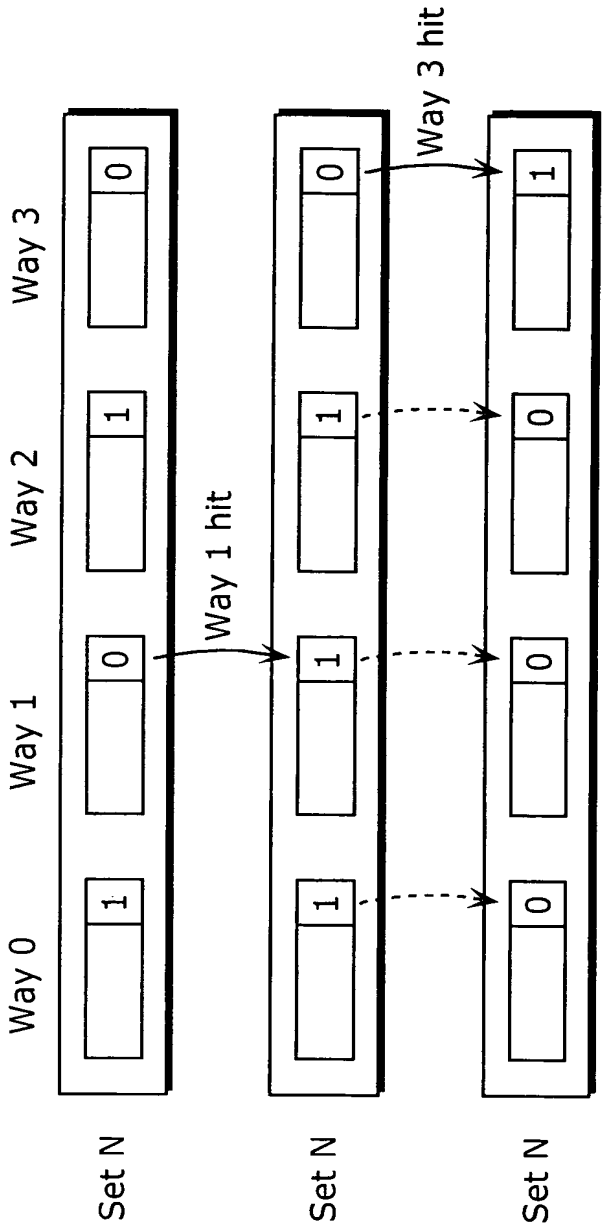
Way 0
Way 1
Way 2
Way 3
Way 1 hit
Way 3 hit
Set N
Set N
Set N
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0
1
0

FIG. 12

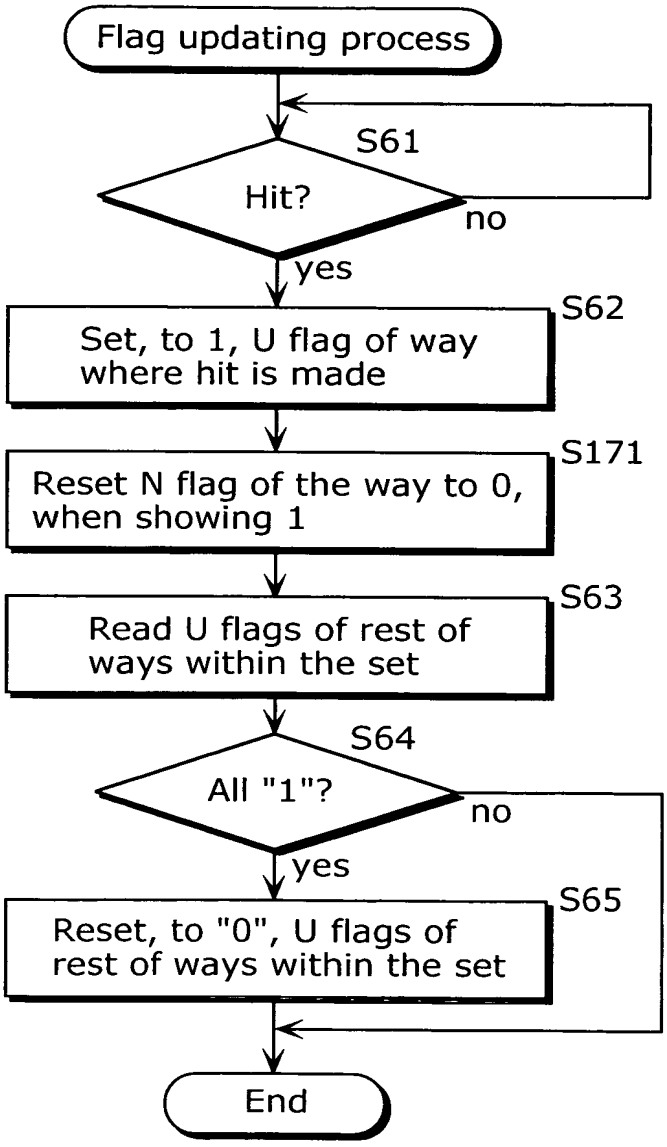
Flag updating process
S61
Hit?
no
yes
S62
Set, to 1, U flag of way where hit is made
S171
Reset N flag of the way to 0, when showing 1
S63
Read U flags of rest of ways within the set
S64
All "1"?
no
yes
S65
Reset, to "0", U flags of rest of ways within the set
End

FIG. 13

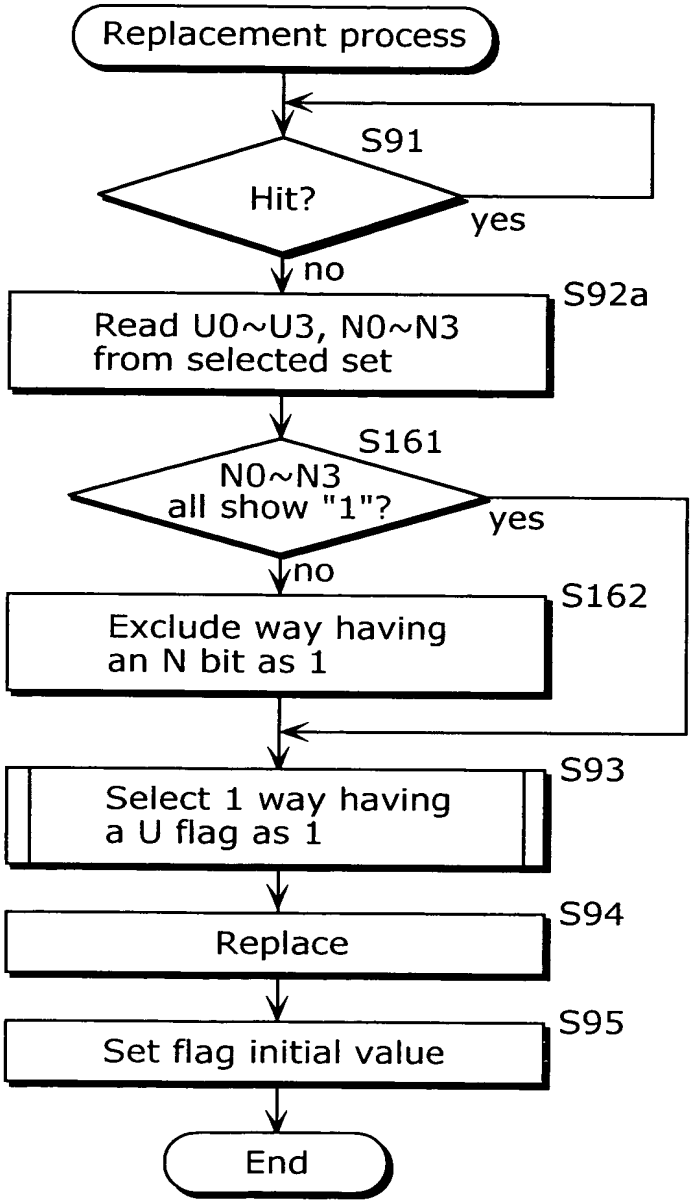
Replacement process
S91
Hit?
yes
no
S92a
Read U0~U3, N0~N3
from selected set
S161
N0~N3
all show "1"?
yes
no
S162
Exclude way having
an N bit as 1
S93
Select 1 way having
a U flag as 1
S94
Replace
S95
Set flag initial value
End

FIG. 14

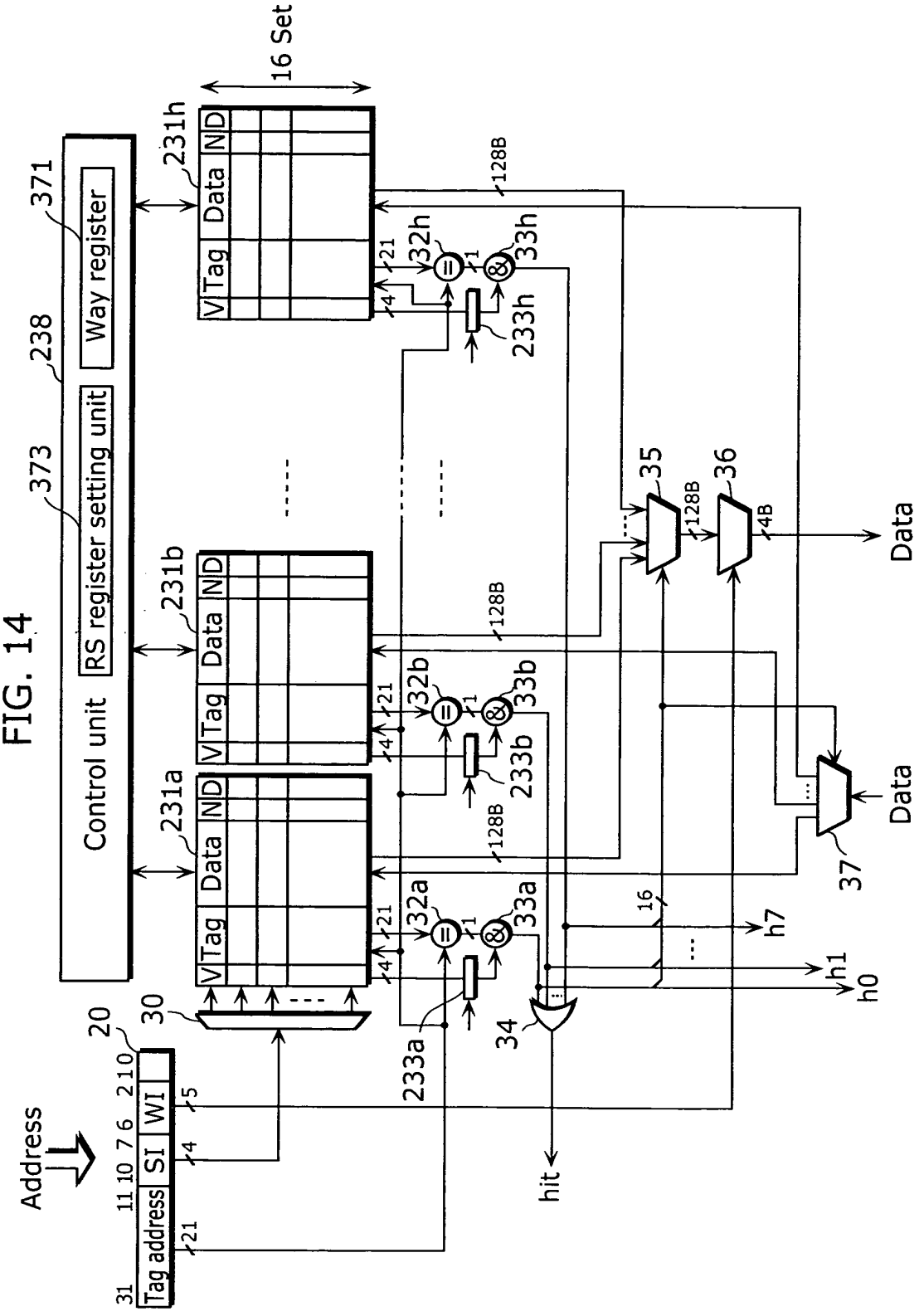
Address
Tag address
SI
WI
Control unit
RS register setting unit
Way register
16 Set
V
Tag
Data
ND
231a
231b
231h
32a
32b
32h
33a
33b
33h
233a
233b
233h
34
35
36
37
hit
h0
h1
h7
Data
128B
4B

FIG. 15

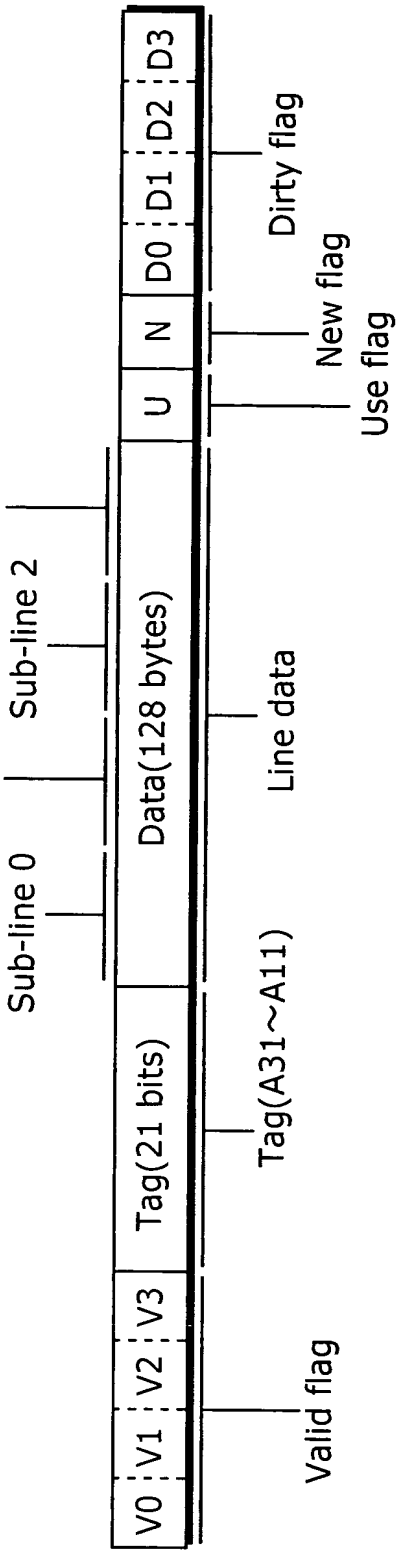
V0
V1
V2
V3
Tag(21 bits)
Data(128 bytes)
U
N
D0
D1
D2
D3
Sub-line 0
Sub-line 1
Sub-line 2
Sub-line 3
Valid flag
Tag(A31~A11)
Line data
Use flag
New flag
Dirty flag

FIG. 16

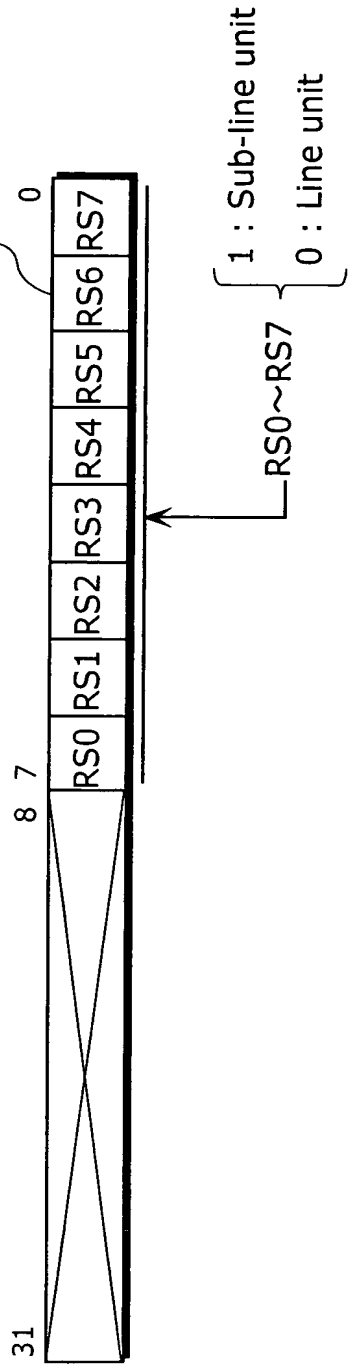
373
0
RS7
RS6
RS5
RS4
RS3
RS2
RS1
RS0
8 7
31
RS0~RS7
1 : Sub-line unit
0 : Line unit

FIG. 17

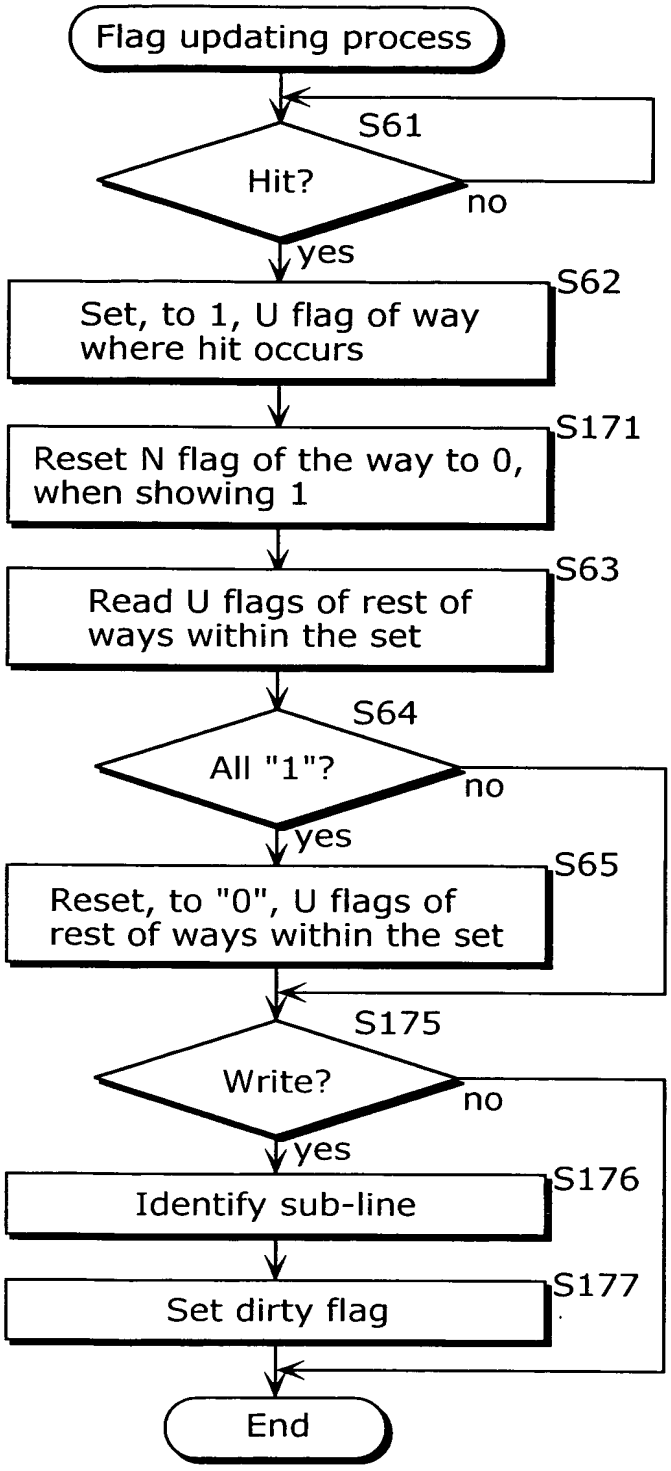
Flag updating process
S61
Hit?
no
yes
S62
Set, to 1, U flag of way where hit occurs
S171
Reset N flag of the way to 0, when showing 1
S63
Read U flags of rest of ways within the set
S64
All "1"?
no
yes
S65
Reset, to "0", U flags of rest of ways within the set
S175
Write?
no
yes
S176
Identify sub-line
S177
Set dirty flag
End

FIG. 18

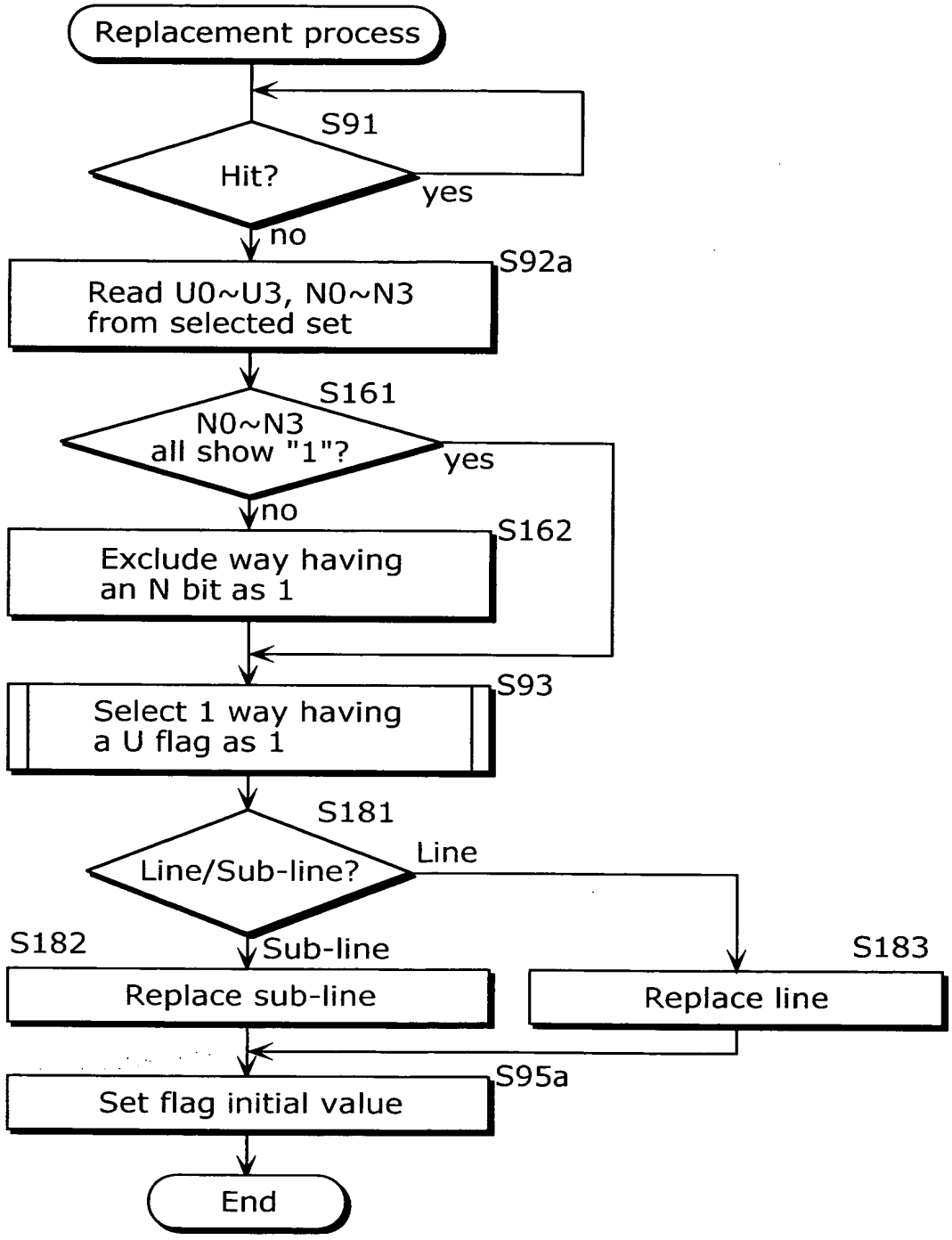
Replacement process
S91
Hit?
yes
no
S92a
Read U0~U3, N0~N3 from selected set
S161
N0~N3 all show "1"?
yes
no
S162
Exclude way having an N bit as 1
S93
Select 1 way having a U flag as 1
S181
Line/Sub-line?
Line
Sub-line
S182
Replace sub-line
S183
Replace line
S95a
Set flag initial value
End

FIG. 19

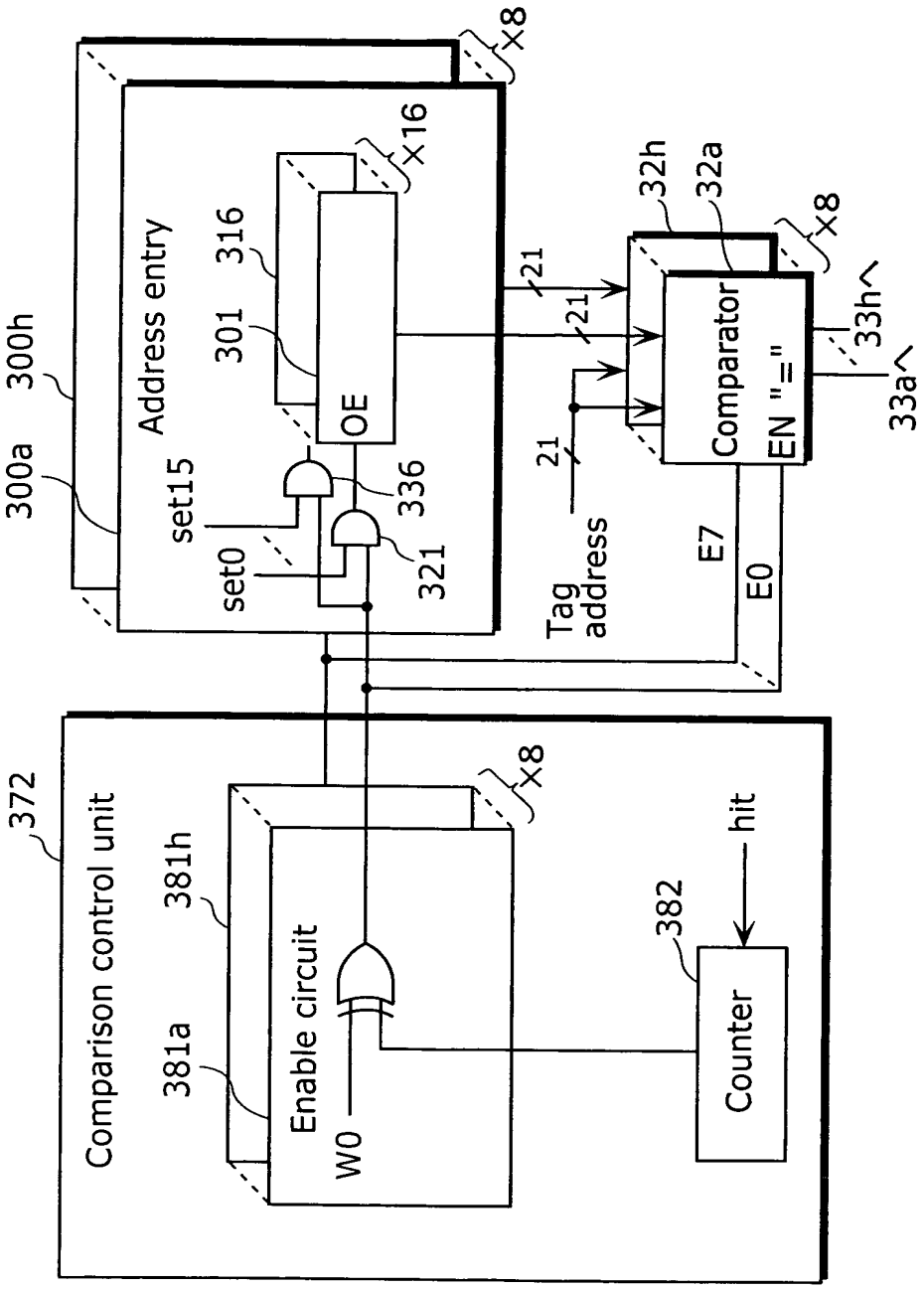
300h
300a
Address entry
set15
set0
316
301
OE
336
321
×16
×8
21
21
21
32h
32a
×8
Comparator
EN "="
33h
33a
Tag address
E7
E0
372
Comparison control unit
381h
381a
Enable circuit
W0
×8
382
Counter
hit

FIG. 20

Input		Output
Wn(n=0~7)	Count value	En
1(Active)	0(First time)	1(Enable)
1(Active)	1(Second time)	0(Disable)
0(Inactive)	0(First time)	0(Disable)
0(Inactive)	1(Second time)	1(Enable)